Figures

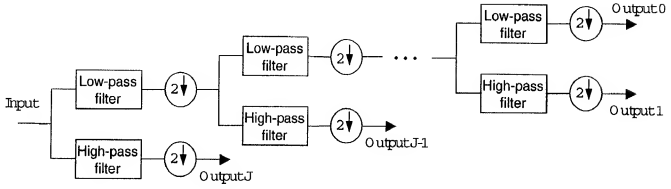


Figure 1. Tree-structured representation of a 1-D discrete wavelet transform

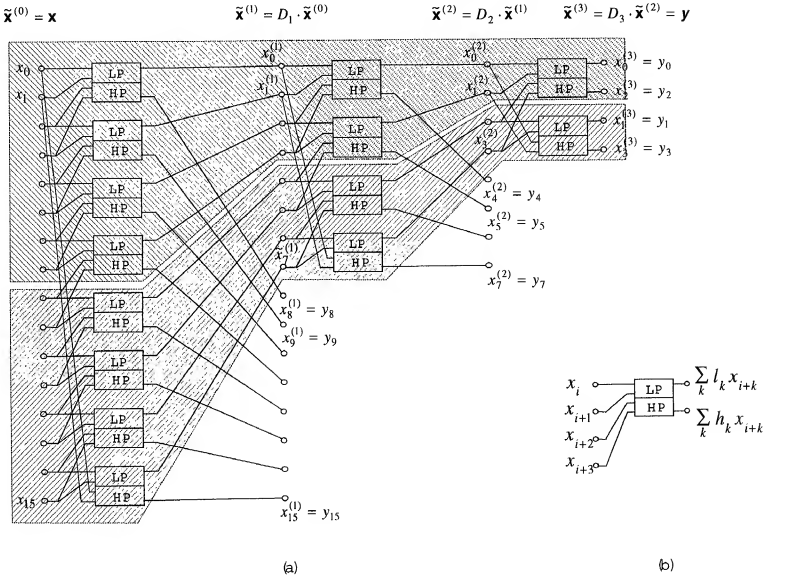


Figure 2. Flowgraph representation of a 1-D discrete wavelet transform ($N=16, L=4, J=3$)

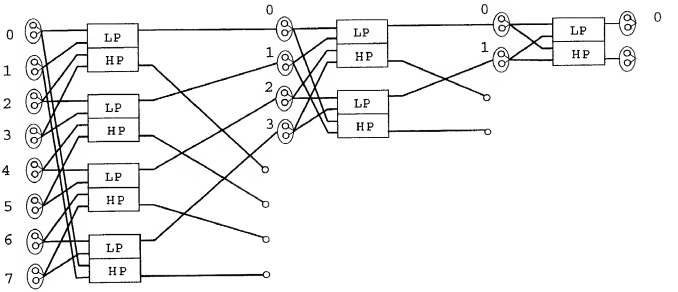


Figure 3. Compact flow graph representation of a 1-D DWT ($L=4, J=3$)

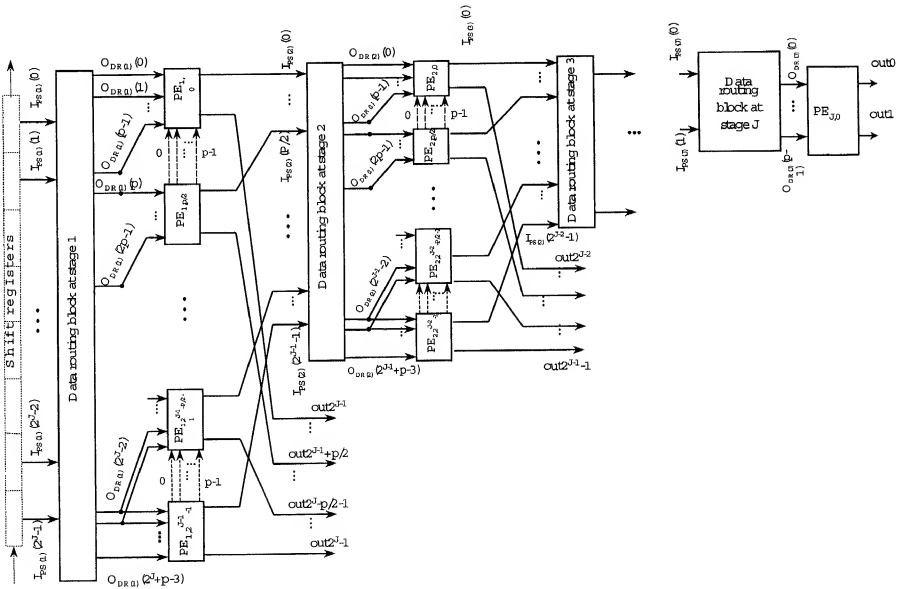


Figure 4. The general structure of Type 1 and Type 2 core DWT architectures

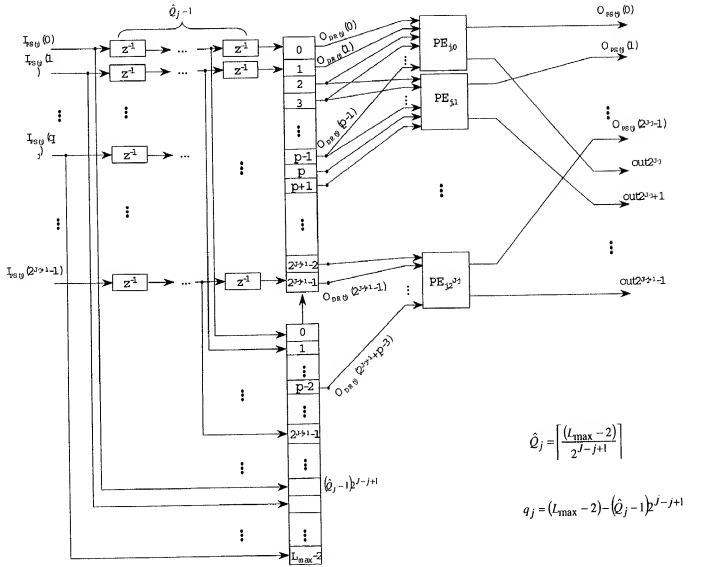


Figure 5. A realization of the jth pipeline stage, $j = 1, \ldots, J$, of the Type 1 core DWT architecture

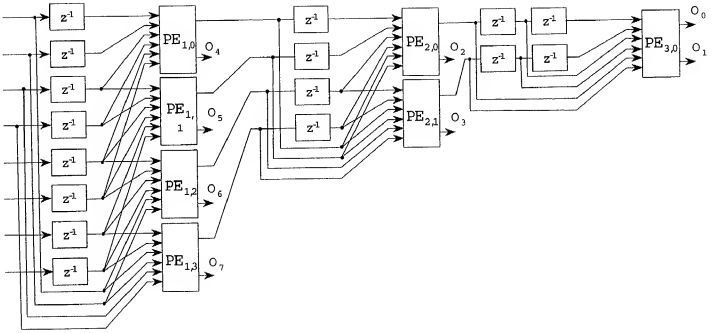


Figure 6. An example of realization of the Type 1 core DWT architecture for the case $P = L_{max} = 6$; $J = 3$; $N = 2^m$, $m = 3,4,...$

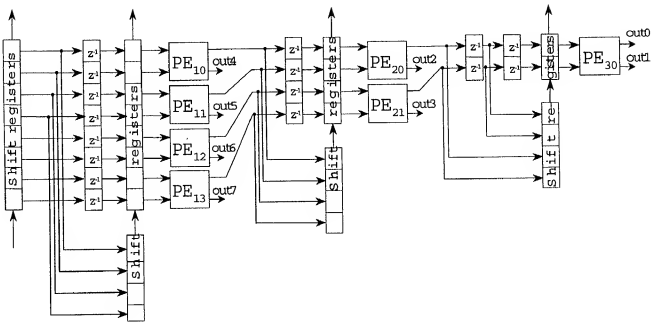


Figure 7. An example of realization of the Type 1 core DWT Architecture for the case $L_{max}=6$; $J_{max}=3$; $p=2$; $N=2^m$, $m=3,4,\ldots$:

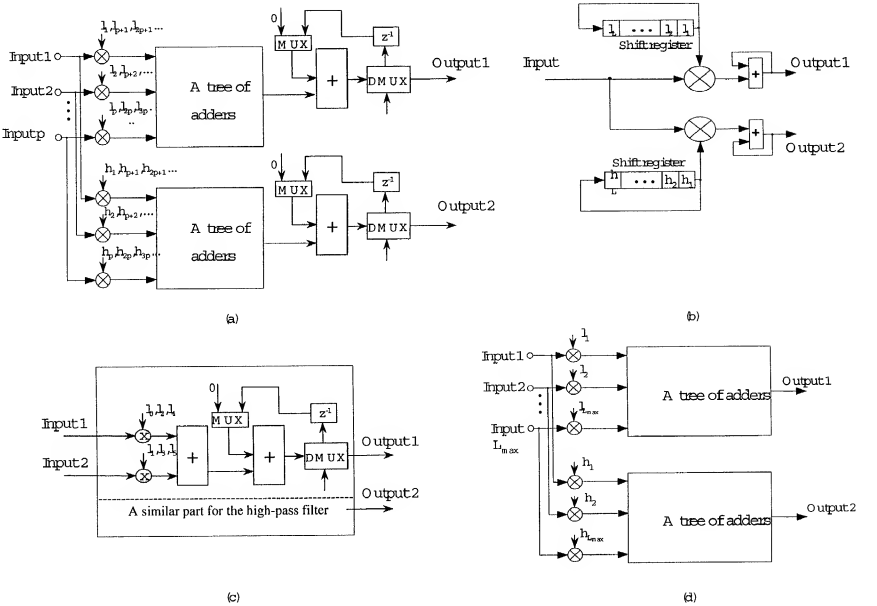
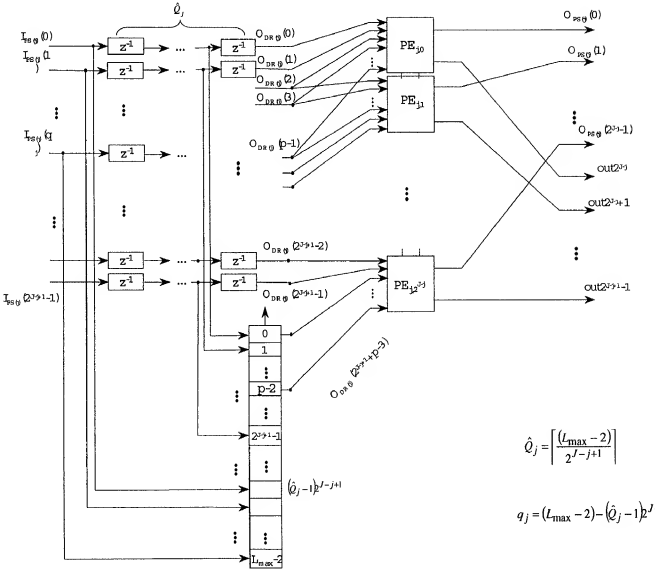


Figure 8. Possible structures for the Pes used in Type 1 core DWT architecture: (a) arbitrary p; (b) p=1; (c) p=2; (d) $p=L_{max}$



$$\hat{Q}_j = \left\lceil \frac{(L_{\max}-2)}{2^{J-j+1}} \right\rceil$$

$$q_j = (L_{\max}-2) - (\hat{Q}_j - 1)2^{J-j+1}$$

Figure 9. A realization of the jth pipeline stage, $j = 1, \ldots, J$, of the Type 2 core DWT architecture

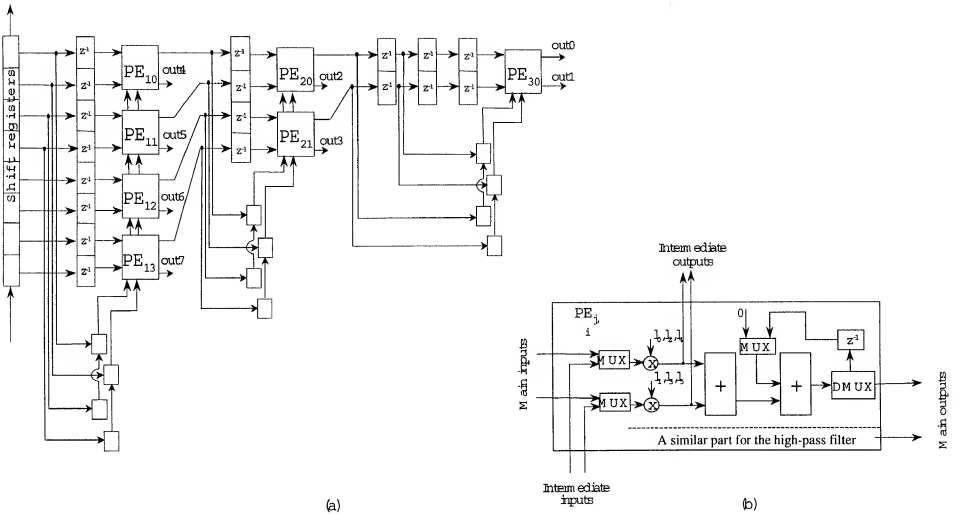


Figure 10. An example of realization of the Type 2 core DWT architecture for the case $L_{max}=6$; $J=3$; $p=2$; $N=2^m$, $m=3,4,\ldots$: (a) the general structure; (b) a possible structure for the PEs.

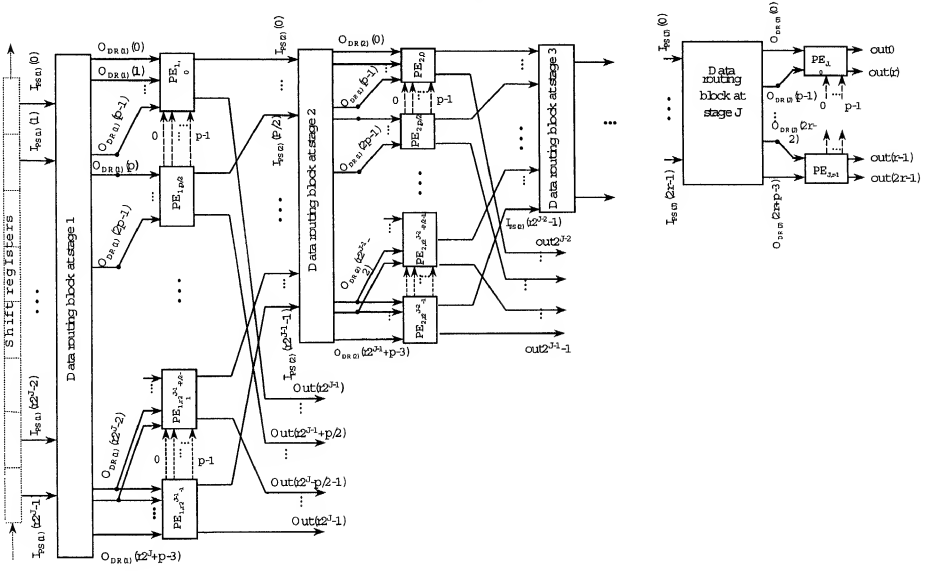
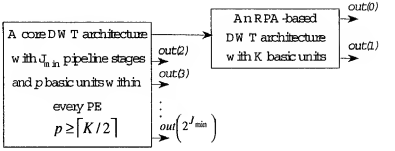
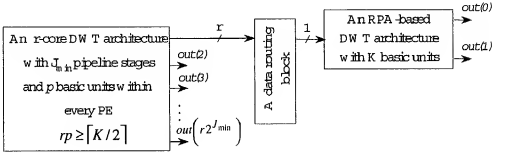


Figure 11. The general structure of multi-core DWT architectures



(a)



(b)

Figure 12. The variable resolution DWT architecture: (a) based on a single-core DWT architecture; (b) based on a multi-core DWT architecture

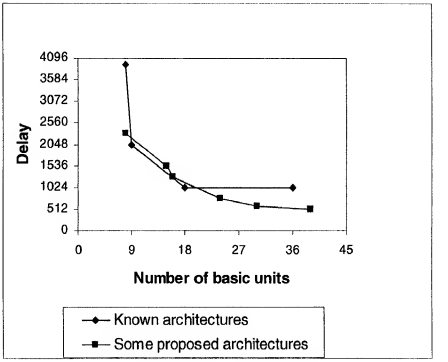


Figure 13. Delay versus number of basic units for some known and proposed DWT architectures (DWT parameters are: $N = 1024, J = 3, L = 9$).

Figure 14.

Table 1. Comparative performance of some DWT architectures

Architecture	Area, A (number of BUs)	Period, T_p	AT_p^2
TMS320C64x [36]	≈ 2 (64-bit)	$4N(1-2^{-J})+25J$	$\approx 32\left(\left(1-2^{-J}\right)N+6J\right)^2$
Architectures in [14], [15]	L	$2N$	$4N^2L$
Architectures in [14]-[19]	$2L$	N	$2N^2L$
Architectures in [12],[24]	JL	N	JN^2L
Architectures of [30]	$4L$ or $\sum_{j=1}^{J}\lceil L/2^{j-2}\rceil$	$N/2$	$\approx N^2L$
FPP DWT [34] (pipelined)	$2NL(1-1/2^J)$	1 (per vector)	$2NL(1-1/2^J)$
LPP DWT [34]	$2L\left(2^J-1\right)$	$N/2^J$	$N^2L(2^J-1)/2^{2J-1}$ $\approx N^2L/2^{J-1}$
Single-core DWT (Type 1 or 2)	$2p\left(2^J-1\right)$	$N\lceil L/p\rceil/2^J$	$\approx N^2p\lceil L/p\rceil^2/2^{J-1}$
Single-core DWT, *p=1*	$2\left(2^J-1\right)$	$NL/2^J$	$\approx N^2L^2/2^J$
Single-core DWT *p=L* $p=L_{max}$ ($L\le L_{max}$)	$2L_{max}\left(2^J-1\right)$	$N/2^J$	$\approx N^2L_{max}/2^{J-1}$
Multi-core DWT	$2pr\left(2^J-1\right)$	$\left(N\lceil L/p\rceil\right)/\left(r2^J\right)$	$\approx\left(N^2p\lceil L/p\rceil^2\right)/\left(r2^{J-1}\right)$
Multi-core DWT, *r=4, p=1*	$8\left(2^J-1\right)$	$NL/2^{J+2}$	$\approx N^2L^2/2^{J+1}$
Multi-core DWT *r=4*, $p=L_{max}$ ($L\le L_{max}$)	$2rL_{max}\left(2^J-1\right)$	$N/\left(r2^J\right)$	$\approx\left(N^2L_{max}\right)/\left(r2^{J-1}\right)$
Variable resolution single-core DWT $p\ge\lceil K/2\rceil$ $(K\le 2L)$	$2p\left(2^{J_{min}}-1\right)+K$ $\approx K2^{J_{min}}$	$N\lceil 2L/K\rceil/2^{J_{min}}$ $\approx 2NL/(K2^{J_{min}})$	$\approx\dfrac{N^2L^2}{K2^{J_{min}-2}}$

Figure 15.
Table 2. Numerical examples from Table 1 (*N=1024, L=9, J=3* and *J=4*)

Architecture	*Number of BUs (gate count)*		*Period, Tp (in cc's)*	
	J=3	*J=4*	*J=3*	*J=4*
TMS320C64x	2 64-bit	2 64-bit		3940
Non-pipelined, [14], [15]	9 (17226)	9 (17226)	2048	2048
Two-stage pipelined, [14]- [19]	18 (34452)	18 (34452)	1024	1024
J-stage pipelined, [12], [24]	27 (51678)	36 (68904)	1024	1024
J-stage pipelined, [30]	36 (68904)	36 (68904)	512	512
FPP DWT (pipelined), [34]	16128 ($3.08 \cdot 10^8$)	17280 ($3.3 \cdot 10^8$)	1	1
LPP DWT (pipelined), [34]	126 (241164)	270 (516780)	64	32
Single-core DWT, p=1	14 (26796)	30 (57420)	1152	576
Single-core DWT, *p=Lmax=10*	140 (267960)	300 (574200)	128	64
Multi-core DWT, r=4, p=1	56 (107184)	120 (229680)	288	144
Multi-core DWT,*r=4,p=Lmax=10*	560 (107184)	1200 (229680)	32	16
Variable resolution single-core DWT, *p=1, (K=2), J_{min}=2*	8 (15312)	8 (15312)	2304	2304
Variable resolution single-core DWT, *p=2, (K=3/K=4), J_{min}=2*	15 (28710) 16 (30624	15 (28710) 16 (30624	1536 1280	1536 1280
Variable resolution single-core DWT, *p=3, (K=6), J_{min}=2*	24 (45936)	24 (45936)	768	768
Variable resolution single-core DWT, *p=5, (K=9), J_{min}=2*	39 (74646)	39 (74646)	512	512

Figure 16.
Table 3. Numerical examples from Table 1 (*N=1024, L=5, J=3* and *J=4*)

Architecture	*Number of BUs (gate count)*		*Period, Tp (in cc's)*	
	J=3	*J=4*	*J=3*	*J=4*
TMS320C64x	2 64-bit	2 64-bit		3940
Non-pipelined, [14], [15]	5 (9570)	5 (9570)	2048	2048
Two-stage pipelined, [14]- [19]	10 (19140)	10 (19140)	1024	1024
J-stage pipelined, [12], [24]	15 (28710)	20 (38280)	1024	1024
J-stage pipelined, [30]	20 (38280) or 15 (28710)	20 (38280) or 18 (34452)	512	512
FPP DWT (pipelined), [34]	8960 ($1.7 \cdot 10^8$)	9600 ($1.8 \cdot 10^8$)	1	1
LPP DWT (pipelined), [34]	70 (133980)	150 (287100)	128	64
Single-core DWT, p=1	14 (26796)	30 (57420)	640	320
Single-core DWT, p=L_{max}=5	70 (133980)	150 (287100)	128	64
Multi-core DWT, r=4, p=1	56 (107184)	120 (229680)	160	80
Multi-core DWT,r=4,p=L_{max}=5	280 (535920)	600 (1148400)	32	16
Variable resolution single-core DWT, *p=1, (K=2), J_{min}=2*	8 (15312)	8 (15312)	1280	1280